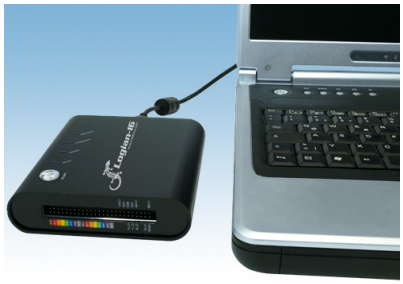
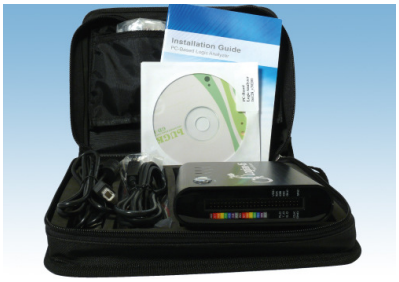
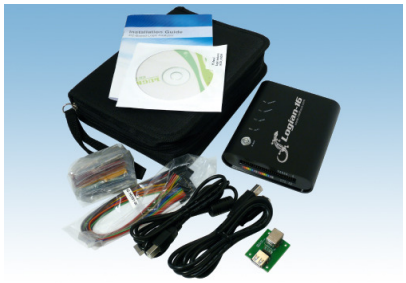
Logian16 Logic analyzer







FEATURES

- PC-based, USB-connected and powered – ideal for portability
- 16 logic channels
- 128kb memory depth / channel
- Compression up to 255:1 depending on activity
- 100 MHz synchronous operation on all channels
- 200 MHz asynchronous operation (16 channels)
- 5 ns glitch capture capability
- Intuitive, easy-to-use Windows application
- Export feature – send to .txt or .csv files for printing / processing
- Timing / State / Single-processor / Bus / Real-time instruction trace analysis
- Flexible signal trigger options (rising/falling/either edge; high, low)
- Hex / Binary / Decimal display formats
- Variable Trigger position (100% pre-trigger to 100% post-trigger, plus up to 16776191 clock cycles of post-trigger delay)
- Channels can be default selected for search or comparison purposes
- Software updates available via CD-ROM or web downloads

ANALYTICS

- I²C Analysis
- UART (RS232C & RS485) Analysis
- Bus Analysis
- Logic Analysis
- Statistic Analysis
- Software Operating Interface

SPECIFICATIONS

- 16 channels
- 100 Hz to 200 MHz sampling frequency
- 256 kb per channel
- External Clock supported
- USB 2.0 interface

INCLUDED ACCESSORIES

- Data Acquisition Module (130 mm x 100 mm x 30 mm, 175 g)
- USB Cable – 1 meter
- 16 channel lead set, plus ground and clock leads
- USB analyzer board
- 20 high-quality test grabbers
- CD-ROM
- User Guide
- Warranty Certificate

Secifications			
Model Type	PC Based Logic Analyzer	Operating systems	Windows (98SE/ME/2000/XP/Vista)
Interface	USB2.0(1.1)	Power	USB
Power Dissipation (running)	1W	Power Dissipation (startup)	2W
Sample rate	Internal clock (Timing Mode) 100Hz~200MHz	Sample rate	External clock (State Mode) 100MHz

	Min	Type	Max
Working Voltage	DC 4.5V	DC 5V	DC 5.5V
Current at Rest			200mA
Current at Work			400mA
Power at Rest			1W
Power at work			2W
Error in Phase Off	- 1.5ns		+ 1.5ns
Vinput of Testing Channels	- DC30V		+ DC30V

Bandwidth	75MHz	Total Memory	4MBits
Memory depth (per channel)	128KBits	Trigger condition	pattern / Edge
Trigger channel	16 channels	Pre/Post trigger	Yes
Trigger level	One level	Trigger count	1~65535
Threshold Voltages	Working range -6V~+6V	Threshold Voltages	Accurate rate -/+ 0.1V
Maximum input voltage	+/- 30V	Impedance	500KΩ/10pF
I2C Protocol	Yes	UART (RS232C & RS485) Protocol	Yes
SPI Protocol	Yes	Data Skew	<1.5ns

Vreference	- DC6V		+ DC6V
Impedance		500KΩ/10pF	
Working Temperature	5 ℃		70 ℃
Storage Temperature	-40 ℃		80 ℃

Special Features
Asynchronous Clock
100MHz asynchronous operation on all channels
Synchronous Clock
100Hz~200MHz synchronous operation on all channels
Memory Depth/channel
128Kbits memory depth/channel
Data Compression
Compression ration of up to 255:1 depending on activity
I2C Protocol Analysis
The I2C, which stands for Inter-Integrated Circuits, is a serial synchronous half-duplex communication protocol. IIC is a synchronous communication protocol and data transmission must be in bytes, a complete IIC signal package must consists of START, ADDRESS, READ/WRITE, DATA, ACK, and STOP segments. The I2C protocol Analysis function is provided.
UART (RS232C & RS485) Protocol Analysis
The UART, which stands for Universal Asynchronous Receiver/Transmitter, is a serial asynchronous protocol. The UART is often time-integrated into PC communication devices, and it usually equips an EEPROM (Electronic Erasable/Programmable Read Only Memory) for error checking proposes with other chips. UART is an asynchronous communication protocol and data transmission may not be in bytes, a complete UART signal package must consists of START, DATA, Parity check, STOP, Buad, and TXD segments. UART (RS232C & RS485) protocol Analysis function is provided.
Bus Protocol Analysis
Bus grouping and Bus protocol analysis functions are provided.
Binary / Decimal / Hexadecimal / ASCII data display formats
Binary / Decimal / Hexadecimal / ASCII data display formats are provided for protocols analysis proposes.
Timing / State / Single-processor / Bus / Real-Time instruction trace analysis
Timing / State / Single-processor / Bus / Real-Time instruction trace analysis functions are provided.
Trigger out function
Trigger out function is provided to synchronous trigger with oscilloscope to measure and decode mixed signals and digital protocols at the same time.
5ns glitch capture capability
5ns glitch capture capability to ensure the accuracy.
Export to TXT or CSV files for processing
The equipment able to export the data into TXT or CSV files for processing.
Flexible signal rigger options
There are rising edge, falling edge, either edge, high and low trigger conditions are provided.
Selectable Trigger position
Selectable trigger position beween 100% pre-trigger and 100% post trigger plus up to 16.7 million clocks of post-trigger delay.
Flexible channels setup state
Channels may be selectively defaulted to "don't care" state.
USB-powered-ideal

USB-powered-ideal for PC and laptops.
Easy-to-use Windows application
Easy-to-use Window (98SE/ME/2000/XP/Vista) application.
Software Updates available
Software updates available from ZEROPLUS website.
16 channels
16 channels to development of MCU applications.
Enable function to filter noise wave or signals
The enable function is provided to filter noise wave or signals.
Statistic Function
The Statistics feature presents user information pertaining to six periodicities: Integrated Periodicities, Positive Periodicities, Negative Periodicities, Eligible Integrated Periodicities, Eligible Positive Periodicities, and Eligible Negative Periodicities.
Customize Interface
Customize interface is provided to modify the display mode, how to modify the ruler mode, how to modify the Bus/Signal Height, and how to modify the background and foreground colors.
SPI Protocol Analysis
SPI (Synchronous Peripheral Interface), is a parallel synchronous full duplex protocol with a bus-like physical interface. This protocol was first developed by Motorola and was generally used for EEPROM, ADC, FRAM, and display device drivers which are devices with low data transmission speeds. The SPI data transmission is synchronous in both receiving and transmitting directions. There are two clocking impulses: CPOL (Clock Polarity) and CPHA (Clock Phase). SPI is a synchronous communication protocol and data transmission may not be in bytes, a complete SPI signal package must consist of SCK, MOSI, MISO, and SS segments with CPHA and CPOL. SPI protocol Analysis function is provided.